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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,503	02/05/2002	Hideki Murayama		4857

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EXAMINER	
THAI, TUAN V	
ART UNIT	**PAPER NUMBER**
2186	3

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,503	MURAYAMA ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-40* is/are pending in the application.

4a) Of the above claim(s) *1* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-17,20-28,30-35 and 37-40* is/are rejected.

7)☒ Claim(s) *18,19,29 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/5/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/227,740/* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Specification

1. This application is a continuation of 09/227,740 filed on January 08, 1999. Claim 1 has been canceled. Claims 2-40 are presented for examination.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

3. The Information Disclosure Statement received 02/05/02 (paper #2) has been fully considered.

Claim Rejections - 35 USC § 112

4. Claims 2-11, 26-27 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 2 and 3, the dependency of these claims are vague and can not be clearly determined since they are depended on the rejected claim 1. The claims are therefore can not be treated under merit at this time. Applicant is required to either cancel the claims or to make proper correction on their

dependency. Claims 4-11 are also rejected since they are depended on the rejected claims 2 and 3.

As per claim 26, the recitation of "form" should be changed to read --from--;

As per claim 27, the recitation of "assigns non-address translated region in said first main memory on memory-mapping of the first main memory" is vague and can not be clearly understood.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 21-28, 30-35 and 37-40 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ninomiya (USPN: 5,764,968).

As per claims 21, 26 and 33; Niomiya teaches the invention as claimed including a computer system supporting a virtual memory system comprising a processor 11 (e.g. see figure 1); a first main memory which said processor 11 accesses is taught as

memory 13 comprises system memory 131 mounted in advance on the system board, and an expanded memory 132 mounted by the user as needed (e.g. see figure 1, column 4, lines 22 et seq.); a non-volatile storage storing configuration information regarding a second main memory to be hot plugged (e.g. see figure 2, column 7, lines 22 et seq.); the processor acquiring the first and second memory information from the non-volatile storage and mapping the first memory based on the first and second memory information (e.g. see column 3, lines 47 et seq.; column 4, lines 59 et seq.; column 9, lines 54 et seq.);

As per claims 22 and 24, wherein the processor generating first logical-physical address translating table for the first memory ... assigning a region to store a second logical-physical address translating table for the second memory in the first memory is embedded in Ninomiya and being taught to the extent that it is being claimed since data being exchanged among memory 131 and modules on the docking station 30 (fig. 2); translation of addresses must occur for data matching; in addition, Ninomiya further discloses system memory 131 having different regions/ modules and wherein the processor accesses the first main memory using first page structure (e.g. see column 4, lines 20 et seq.);

As per claim 23, different pages structure associated with different memory modules having at least one bank, and the untranslatable/translatable region being corresponded to the

used/unused RAS lines for unused/used banks (e.g. see column 9, lines 29 bridging column 10, line 30);

As per claim 25, Ninomiya clearly discloses the nonvolatile memory 34 is an EEPROM (e.g. see figure 2; column 7, lines 23 et seq.);

As per claim 27, Ninomiya discloses the non-translated/ translatable region being corresponded to the used/unused RAS lines for unused/used banks (e.g. see column 9, lines 29 bridging column 10, line 30);

As per claim 28; Ninomiya discloses the system BIOS checks the size of banks connected to the RAS lines by write/read comparison or the like to detect unused banks (e.g. see column 10, lines 23 et seq.);

As per claim 30, Ninomiya discloses the non-address translated region being corresponded to the unused RAS lines for unused/used banks wherein the unused RAS lines are determined by the number of RAS lines prepared for the system memory 131 and the expanded memory 132 and the bank structure of the actually mounted memory module (e.g. see column 9, lines 29 bridging column 10, line 30);

As per claim 31, Ninomiya clearly discloses the nonvolatile memory 34 is an EEPROM (e.g. see figure 2; column 7, lines 23 et seq.);

As per claim 32, the TLB within the processor is embedded in the system of Ninomiya since data being exchanged among memory 131 and modules on the docking station 30 (fig. 2); translation of addresses must occur for data matching; in addition, Ninomiya further discloses system memory 131 having different regions/ modules and wherein the processor accesses the first main memory using first page structure (e.g. see column 4, lines 20 et seq.);

As per claims 34-35 and 37-40, they encompass the same scope of invention as to that of claims 27-28 and 30-32; the claims are therefore rejected for the same reasons as being set forth above; noting that the top priority region being the same as the non-address translated region and is equivalent to the unused RAS lines for unused/used banks wherein the unused RAS lines are determined by the number of RAS lines prepared for the system memory 131 and the expanded memory 132 and the bank structure of the actually mounted memory module (e.g. see column 9, lines 29 bridging column 10, line 30);

Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 12-17 and 20 are rejected under 35 U.S.C. § 103 as being unpatentable under Dhuey (USPN: 4,926,314) in view of Sykora (USPN: 4,860,252);

As per claims 12-13, 15-17 and 20; after close analysis, the current invention is directed to an information processing apparatus and method for allowing a memory to be added (expansion) thereto while be powered; and numerous references can be used as prior art, and accordingly, the prior arts of Dhuey and Sykora were chosen by the Examiner because they clearly demonstrate the concept of the current invention. For example, Dhuey, in his teaching of method and apparatus for determining available memory size, discloses the invention as claimed including a memory managing method for use with an information processing apparatus comprising first memory 18, an a processor 10 for processing information held in the first memory 18, the information processing apparatus further allowing second memory 20 to be added thereto (e.g. see figure 1), the memory managing method comprising the steps of: connecting the processor to at least one of the first and second memory (e.g. see figure 1); storing the sizes of the first and second memories connected to the processor and storing information about whether or not each of the first and second memories is connected to the processor (e.g. see column 1, lines 34 et seq.; column 2, lines 20 et seq.; column 4, lines 21 et seq.); establishing a total memory size,

calculating the actually installed memory ... are further taught by Dhuey as the CPU repeats this procedure for the next bank of memory until the total available memory of the system is determined. A bit value is assigned which corresponds to the available memory size of the first memory bank. This bit value is stored in a register coupled to control logic which controls the operation of the multiplexor and generates row address (RAS) and column address (CAS) signals to access the memory, and memory banks are selected by the control logic based upon the logical state of predetermined address bits outputted by the CPU which are identified by the bit value (e.g. see abstract, column 2, lines 18 et seq.; column 7, lines 9 et seq.);

Dhuey, however does not particularly teaches the concept of "hot insertion/removal" of the first and second memory while the system being powered;

It should be noted that the "hot insertion/removal" of memory module while powering-up is well known in the memory storage art; for example, Sykora, in his teaching of self-adaptive computer memory address allocation system, clearly discloses that memory modules can be added to the system during powered up, the system detects the presence of the memory connected to the memory banks of a plurality memory modules, the system further receives and remaps the address signal, noting that the remapping process is performed during the power up; by

doing so, Sykora teaches that it would allow for faster memory accessing since no wait states are introduced during subsequent memory accesses (e.g. see abstract, column 1, line 62 bridging column 2, line 54). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the "hot insertion/removing of memory modules" as being taught by Sykora for that of Dhuey system, since Sykora clearly discloses that it would allow for faster memory accessing since no wait states are introduced during subsequent memory accesses; therefore being advantageous (e.g. see abstract, column 1, line 62 bridging column 2, line 54). By this rationale, claims 12-13, 15-17 and 20 are therefore rejected.

As per claim 14, it should be noted that computer monitor is known to be integral and embedded in any nowadays computer system, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to display the size of memory added or the expandable memory size in order to provide any users with a quicker reference, therefore allowing the combined Dhuey and Sykora's system to operate with a more friendly user interface;

Allowable subject matter

7. Claims 18-19, 29 and 36 are objected to as being dependent

upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims.

Conclusion

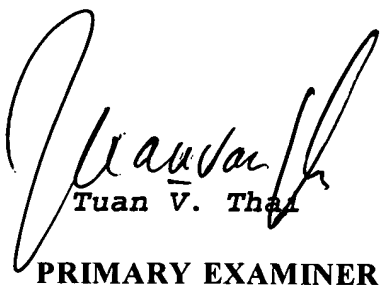
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is 703-305-3842.

The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew M. Kim can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900. The official phone fax number for the group is 703-872-9306.

TVT/November 24, 2003



Tuan V. Thai

PRIMARY EXAMINER

Group 2100